REMARKS

The Examiner is thanked for the due consideration given the application.

Claims 33-63 are pending in the application. Claim 33 has been amended to better set forth the invention being claimed.

No new matter is believed to be added to the application by this amendment.

Rejection Under 35 USC §112, Second Paragraph

Claims 33-35 and 37-60 have been rejected under 35 USC §112, second paragraph, as being indefinite. This rejection is respectfully traversed.

The comments regarding claim 33 have been considered, and claim 33 has been appropriately amended.

The Official Action asserts that the term "the common processor" in claim 34 lacks antecedent basis. However claim 33, from which claim 34 depends, recites the term "a common processor" in the last two lines of the claim.

The claims are thus clear, definite and have full antecedent basis.

This rejection is believed to be overcome, and withdrawal thereof is respectfully requested.

Rejections Over OCHS et al.

Claims 33-41, 43, 47, 51, 53, 54, and 58-63 have been rejected under 35 USC §102(b) as being anticipated by or, in the alternative, under 35 USC §103(a) as unpatentable over OCHS et

al. (U.S. Patent 5,899,925). Claims 42, 44-46, 48-50, 52 and 55-57 have been rejected under 35 USC §103(a) as being unpatentable over OCHS et al. These rejections are respectfully traversed.

The present invention provides a system in which the components making up a medical device each has its own self-test means which is activated independently of the main device processor.

There are several advantages associated with this autonomous type of operation. In the arrangement of the present invention, the main processor of the device merely has to look at the results of the self-test only; it does not have to receive and transmit control or other information to the individual component for the purposes of obtaining test results. This therefore lightens the load on the central processor unit.

Also, the system is particularly useful during assembly of a medical device because it enables the components of the device to be self-tested prior to and during assembly. This means that a faulty component can be detected at an early stage rather than only when the entire medical device has been assembled.

By having each component have its own test facility the arrangement is fault tolerant. In the arrangement of OCHS et al., having a single controller testing several different components means that if the controller fails, the failure is not obvious to the main processor, and furthermore no test an be carried out.

In the autonomous arrangement as claimed, if one controller fails it is more obvious and also the remaining tests can still be carried out and so there is built in redundancy.

The present invention is typically illustrated, by way of example, in Figure 3 of the application, which is reproduced below.

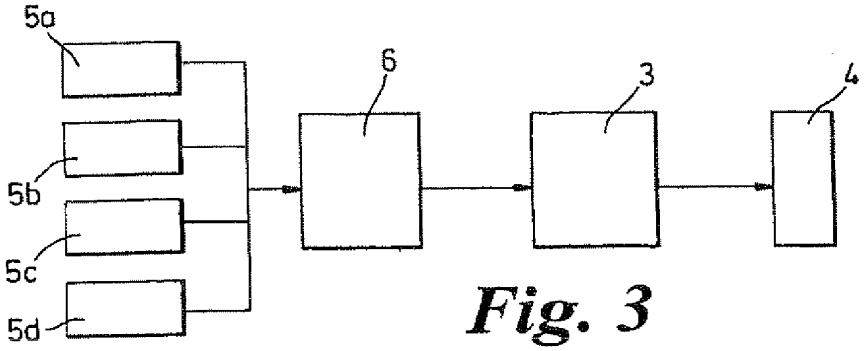

Fig. 3

As shown in Figure 3 (and has been discussed in the previous response), data from the individual components 5(a) to 5(d) is fed as an output from test circuits for the individual components, and these are fed to a communication output as a collated signal, which passes to the summator 6. Information from the summator is then fed by a communication link to a processor 3, and the central processing unit in the processor collates the information from the summator with stored memory data concerning the components being tested. A single communication link sends an output to the indicator 4, for example a digital display, to show the status of the combined data from the components 5(a) to 5(d).

Looking more specifically at OCHS et al., and in particular the passage on column 3, lines 47-59, it is stated that the system monitor generates a test signal to initiate testing of defibrillator functions. In that arrangement it is therefore clear that the responsibility for testing of the various components is controlled centrally at the system monitor. Also, OCHS et al. then state that the system monitor applies the test signals to the CPU (that is the main controller of the device) with the CPU controlling and gathering information from the various tested defibrillator components. In other words, it is clear that that a periodic timing of the various tests is controlled by the system monitor but otherwise the remaining test functions are carried out by the CPU 16.

These features of OCHS et al. can be better understood by referring to Figure 2 of the reference, which is reproduced below.

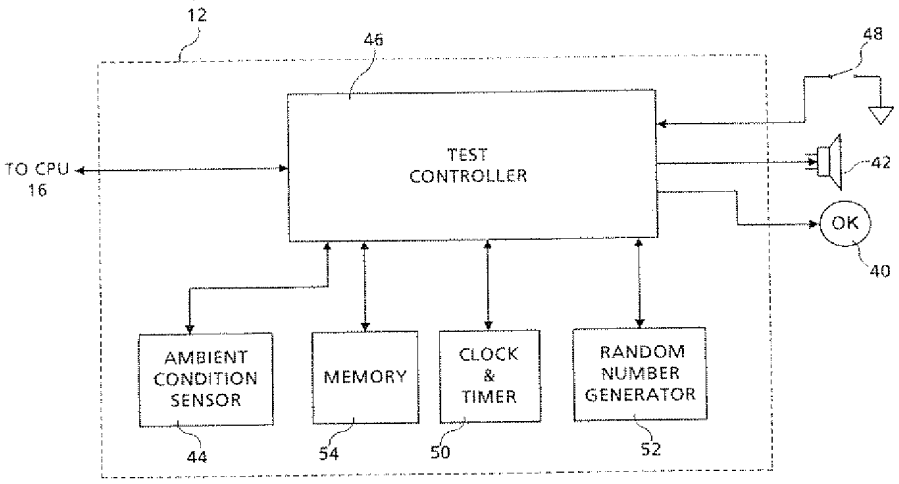

FIG. 2

At column 3, lines 60 to column 4, line 9, OCHS et al. state that the various components may contain circuitry for testing and communicating component status to the CPU 16 and the system monitor 12. For example, the ECG circuit 24 (see Figure 1, reproduced below) may include a signal generator for generating test ECG signals to test ECG amplifier and analogue - to-digital converter functions.

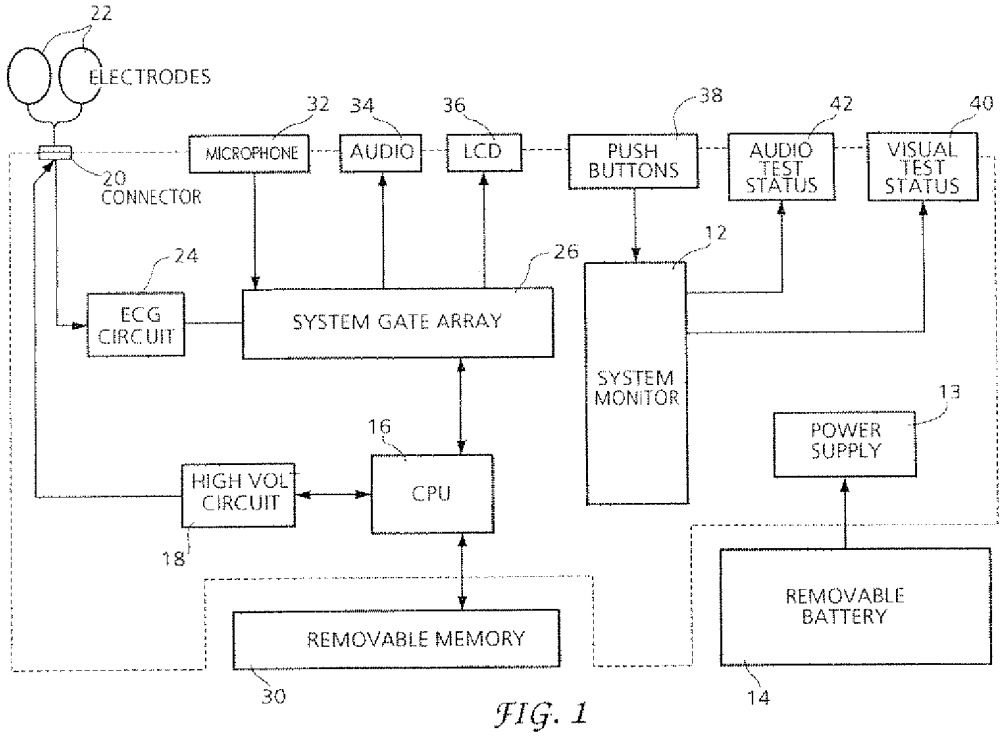

FIG. 1

The Office's position that this operation is activated independently of operation of the medical device is clearly in error. The signal generator of OCHS et al. generates a test ECG signal and not an activation signal. Where the signal generator is to be an activation signal generator a second ECG test signal generator will be required to further conduct the test, and no

such provision exists. OCHS et al. clearly intended the signal generator to simulate an ECG signal similar to that produced by the human heart in order to test the operations of the ECG circuitry. OCHS et al. does not teach this signal generator being self-activated. On the contrary, OCHS et al. teach the activation signals are borne from centralized system monitor 12.

Additional distinctions of the present invention over OCHS et al. were set forth in the response filed November 28, 2007. For brevity, these distinctions are not repeated here.

As a result, OCHS et al. fail to anticipate or render *prima facie* unpatentable the structures and functions set forth in independent claims 33, 36 and 61. Claims depending upon these independent claims are patentable for at least the above reasons.

These rejections are believed to be overcome, and withdrawal thereof is respectfully requested.

Conclusion

The prior art of record but not utilized is believed to be non-pertinent to the instant claims.

The Examiner is thanked for initialing the supplemental PTO-1449 form.

The rejections are believed to have been overcome, obviated or rendered moot, and no issues remain. The Examiner is accordingly respectfully requested to place the application in condition for allowance and to issue a Notice of Allowability.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON

Robert E. Goozner, Reg. No. 42,593
209 Madison Street
Suite 500
Alexandria, VA 22314
Telephone (703) 521-2297
Telefax (703) 685-0573
(703) 979-4709

REG/fb